Validating an LPDDR4 Memory Interface with Multiple Frequencies and Gated Clock Intervals

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Abstract and Takeaways

The LPDDR4 memory specification has been published by JEDEC. It targets high performance mobile and handset applications with data rates reaching 4267 MT/s. LPDDR4 memory also supports aggressive power management capabilities, such as real-time frequency switching and gated clocking. Validating an LPDDR4 interface with the power management capabilities fully enabled, presents a challenge for analysis equipment. In this session, unique analysis techniques are shown to report multi-frequency protocol compliance and statistics, as well as utilization comprehending clock gated intervals at full specified data rates.

1. The advanced power management techniques used on LPDDR4 memory interfaces can utilize multiple bus clock frequencies and intervals when the clock is gated off. These power management techniques will often be the focus of validation and debug efforts.

2. Typical analysis techniques may not be applicable to these types of validation and debug challenges.

3. Enhanced analysis techniques are being developed to address these challenges.
Outline

- **LPDDR4 overview**
  - Optimized for bandwidth AND power management
  - Published spec and highlighted areas

- **Validation challenges**
  - Clock stoppage
  - Frequency switching

- **Solution paths**
  - Parameters and frequency dependencies
  - Interconnect and probing
  - Real-time timing measurements
  - Acquiring performance data
Overview of Bandwidth and Power Management

- **PC Client**
  - PC DRAM
  - x128 (2ch x64)
  - Module

- **LPDDR4**
  - 51.2GB/s
  - (128 IO * 3.2Gbps)

- **DDR4**
  - 38.4GBps

- **Smart Phone**
  - Mobile DRAM
  - x64 (6ch x32)
  - 1 PKG

- **Portable Client/ Tablet PC/ Super Phone**
  - 25.6GBps
  - (64 IO * 3.2Gbps)

**LPDDR4 Energy Efficiency**

- LPDDR1: 1X
- LPDDR2: 0.64X (-36%)
- LPDDR3: 0.58X (-10%)
- LPDDR4: 0.36X (-37%)

Energy efficiency measures power consumption per bandwidth.
LPDDR4 Spec Highlights

- JEDEC published the LPDDR4 spec, JESD209-4 in August, 2014
- Unique power management features
  - Clock Stop Flexibility
  - Duplicate MRs enable dynamic tCK and freq
  - Unlimited # of FSP MR value sets

<table>
<thead>
<tr>
<th>Performance/Power Mode</th>
<th>Low Power</th>
<th>High Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Set Point</td>
<td>FSP0</td>
<td>FSP1</td>
</tr>
</tbody>
</table>

*Figure 59 — Switching to a Third Trained Frequency Set-Point*
Resulting Measurement Challenge
Analyzing Across a Frequency Switch

- **Protocol Compliance**
  - Continuous monitoring of protocol sequences
  - Pass/fail thresholds by frequency

- **Utilization and Throughput**
  - Identifying frequency set points applied
  - Determining and measuring performance thresholds for combinations of frequency set points
Protocol Parameter Thresholds vs. Frequency

- Protocol pass/fail thresholds vary by frequency:
  - Parameters with nCK units vary in time intervals
  - Parameters with nS units vary in multiples of clocks
  - In some cases, checks for both may be required

### Table 62 — Power-Down AC Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min/Max</th>
<th>Data Rate</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Down Timing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Valid Clock and CS Requirement after CKE Input low after MRW Command</td>
<td>tMRWCKEL</td>
<td>Min</td>
<td>Max(14ns, 10nCK)</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command</td>
<td>tZQCKE</td>
<td>Min</td>
<td>Max(1.75ns, 3nCK)</td>
<td>ns</td>
<td>1</td>
</tr>
</tbody>
</table>

- The range of frequencies needs to be considered for each parameter

### Table 7 — Equations

<table>
<thead>
<tr>
<th>Clk / nS</th>
<th>Param Name</th>
<th>Equation</th>
<th>Parameter 1</th>
<th>Parameter 2</th>
<th>Parameter 3</th>
<th>Parameter 4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>tCKMHz</td>
<td></td>
<td>100</td>
<td>400</td>
<td>800</td>
<td>1600</td>
</tr>
<tr>
<td></td>
<td>tCKns</td>
<td>$1/tCKMHz * 1000$</td>
<td>10.00</td>
<td>2.50</td>
<td>1.25</td>
<td>0.63</td>
</tr>
<tr>
<td></td>
<td>tNCxChRTW16</td>
<td>$RL + Round(tDQSCKmax/tCKns) + 8 - WL + tWPRE + tRPST$</td>
<td>11</td>
<td>12</td>
<td>14</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>tRRD</td>
<td>max(10, 4*tCKns) + tNCxTempDerating</td>
<td>40</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>tFAW</td>
<td></td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
</tr>
</tbody>
</table>
More Measurement Challenges

- LPDDR4 commands can extend over 1, 2 or 4 clock cycles.

- The command stream interleaves 1, 2 and 4 cycle commands as needed.

- Real-time timing measurements are required which combine
  - Clock synchronous state sampling, typical in any logic analyzer
  - Real-time decoding of the command stream protocol
  - Time intervals measured independently of the LPDDR4 interface clock
  - ...at 2.1GHz clocking
Solution Part 1 - Probing and Interposers

- The probing system is designed to have minimal impact on the target.
- Interposers meet the performance demands of the memory bus max frequency to enable continuous analysis and validation.
Solution Part 2 – LPDDR4-Aware Analysis System

- Programmable Front-End
- Logic Analyzer
- Real-Time Protocol Analyzer
- Results & Captures
Test Cases Employing a Pattern Generator
Test Pattern: 3 Frequencies & Clock Stops in PDE/PDX

REGION A 1600MHZ:
ACT 0
READ 0
PRE0
PDE

REGION B 800MHZ
PDX
ACT 0
READ 0
PRE0
PDE

REGION C 533MHZ
PDX
ACT 0
READ 0
PRE0
PDE

REGION D 1600MHZ
PDX

REGION X – CLOCK STOPPAGE
Multi-frequency characterization

- The analyzer enables the user to select “Session Setups” which establishes the type of measurements.

- “Timebase Measurement” scans the bus and identifies the clocking frequencies that are present.
The analyzer’s programmable front end can be used as a digital sampling scope, graphically displaying signal eyes.

In multi-frequency traffic, the left edge of each clock period aligns to the reference clock edge.

A multi-frequency eye is formed, with an eye size associated with the shortest clock period.
Multi-frequency signal eyes taken from a live target

The memory controller is switching between frequencies based on loading algorithms, creating a pseudo random frequency pattern
Real-time protocol statistics & timing measurements

- Spec thresholds are set for the combined frequency set.
- Screen continuously updates protocol check results.
- Acquisitions enable timing measurements with cursors.
Performance Measurements

- Continuously Accumulating Statistics
- Sampling enables real-time charting of performance measures
- Acquisition based performance measures enable timestamp level resolution
Ex: Clock Stopped Interval Time Measurement

- Analyzer can trigger on a PDE/PDX containing a clock stoppage
- Selectable elapsed time values
  - < minimum
  - > maximum

![Image of analyzer interface with clock stopped measurement example]
Ex: Time Spent in Power-downs; Including Clock Stops

- Storage can be qualified to capture power-down events.
- The acquisition can be filtered and exported in .csv format.

<table>
<thead>
<tr>
<th>Mark</th>
<th>Sample</th>
<th>Timestamp (ns)</th>
<th>Elapsed (ns)</th>
<th>Command Rank 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9,998,531</td>
<td>72,331,890.88</td>
<td>604.00 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>2</td>
<td>9,995,696</td>
<td>72,333,108.00</td>
<td>414.63 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>3</td>
<td>9,998,821</td>
<td>72,333,872.38</td>
<td>210.63 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>4</td>
<td>9,998,967</td>
<td>72,335,016.38</td>
<td>604.00 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>5</td>
<td>9,999,124</td>
<td>72,336,233.00</td>
<td>414.13 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>6</td>
<td>9,999,249</td>
<td>72,336,996.88</td>
<td>210.13 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>7</td>
<td>9,999,395</td>
<td>72,338,140.88</td>
<td>604.00 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>8</td>
<td>9,999,560</td>
<td>72,339,350.00</td>
<td>414.63 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>9</td>
<td>9,999,685</td>
<td>72,340,122.38</td>
<td>210.63 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>10</td>
<td>9,999,898</td>
<td>72,341,266.38</td>
<td>604.00 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
<tr>
<td>11</td>
<td>9,999,988</td>
<td>72,342,470.50</td>
<td>402.58 ns</td>
<td>EXIT POWER DOWN</td>
</tr>
</tbody>
</table>

- Acquired Bus Time: 72,342,470.50 ns
- Sum of all Powerdown time: 28,443,270.63 ns
- Total productive bus time: 43,899,199.87 ns
Ex: Time Spent at Frequency by Acquisition Analysis

- Exported acquisitions show the clock period in the cycle-to-cycle elapsed time.
- Adjacent PDEs can be compared to determine if a frequency switch occurred.
- Delta of the associated timestamps equals the time spent at that frequency.
Summary

- Unique validation challenges of LPDDR4 have been highlighted
  - Aggressive use of power management features
  - Multi-cycle commands of 1, 2 or 4 cycles, interleaved
  - High data rates; 2133MHz clock

- A solution to address these challenges employs a combination of both clock synchronous and non-synchronous measurements

- Work continues to automate performance measurements to address LPDDR4 implementation paths