DRAM in the Automobile: What, Where, Why, and How
Marc Greenberg
Director, Product Marketing, DDR and AMBA IP
Synopsys

marc.greenberg@synopsys.com
Legal Notice

This presentation is intended as a DDR Memory technology guide and is not intended as a guide to Synopsys products.

Information contained in this presentation may or may not reflect Synopsys products or plans as of the date of this presentation. If plans exist, such plans are subject to completion and are subject to change.

Products may be offered and purchased only pursuant to an authorized quote and purchase order.
Abstract

• There are now hundreds of microprocessors in most new automobiles, from simple sensor/actuator controllers to sophisticated engine control computing functions. While every processor needs to have some memory, traditionally on-chip SRAM has been used to service the needs of these processors.

• New applications like Advanced Driver Awareness Systems (ADAS), multi-camera vision processing, improved infotainment, and self-driving automobiles have computing demands on memory that cannot be met using on-die SRAM alone, and it’s now a requirement to have some DRAM in these types of systems.

• Since DRAM is new in the automobile, there are many questions that designers have about DRAM, such as the types and arrangements of DRAM that are most suitable for new designs, how DRAM can survive the automotive environment, how to address automotive reliability, and how to address automotive quality.
Introduction

• Automotive semiconductors have traditionally been found in two areas:
  – Safety-critical: engine management, ABS braking, cruise control, dashboard
    – Modest compute requirements well served by SRAM
  – Non-safety critical: radio, navigation, DVD player, communication, backup camera
    – When image processing is required, larger capacity DRAM is often needed
• Advanced Driver Awareness Systems (ADAS) put DRAM into safety-critical components:
  – Systems based on Embedded Vision
    – Collision Warning / Avoidance / Braking
    – Pedestrian Warning / Avoidance / Braking
    – Lane Departure Warning
  – Fully autonomous vehicles
    – Specific tasks (highway driving, parking)
    – All tasks to move vehicle from A to B
# SAE 6 Levels of Autonomous Driving

<table>
<thead>
<tr>
<th>SAE level</th>
<th>Name</th>
<th>Narrative Definition</th>
<th>Execution of Steering and Acceleration/Deceleration</th>
<th>Monitoring of Driving Environment</th>
<th>Fallback Performance of Dynamic Driving Task</th>
<th>System Capability (Driving Modes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human driver monitors the driving environment</td>
<td>No Automation</td>
<td>the full-time performance by the human driver of all aspects of the dynamic driving task, even when enhanced by warning or intervention systems</td>
<td>Human driver</td>
<td>Human driver</td>
<td>Human driver</td>
<td>n/a</td>
</tr>
<tr>
<td>0</td>
<td>Driver Assistance</td>
<td>the driving mode-specific execution by a driver assistance system of either steering or acceleration/deceleration using information about the driving environment and with the expectation that the human driver perform all remaining aspects of the dynamic driving task</td>
<td>Human driver and system</td>
<td>Human driver</td>
<td>Human driver</td>
<td>Some driving modes</td>
</tr>
<tr>
<td>2</td>
<td>Partial Automation</td>
<td>the driving mode-specific execution by one or more driver assistance systems of both steering and acceleration/deceleration using information about the driving environment and with the expectation that the human driver perform all remaining aspects of the dynamic driving task</td>
<td>System</td>
<td>Human driver</td>
<td>Human driver</td>
<td>Some driving modes</td>
</tr>
<tr>
<td>Automated driving system (&quot;system&quot;) monitors the driving environment</td>
<td>Conditional Automation</td>
<td>the driving mode-specific performance by an automated driving system of all aspects of the dynamic driving task with the expectation that the human driver will respond appropriately to a request to intervene</td>
<td>System</td>
<td>System</td>
<td>Human driver</td>
<td>Some driving modes</td>
</tr>
<tr>
<td>3</td>
<td>High Automation</td>
<td>the driving mode-specific performance by an automated driving system of all aspects of the dynamic driving task, even if a human driver does not respond appropriately to a request to intervene</td>
<td>System</td>
<td>System</td>
<td>System</td>
<td>Some driving modes</td>
</tr>
<tr>
<td>4</td>
<td>Full Automation</td>
<td>the full-time performance by an automated driving system of all aspects of the dynamic driving task under all roadway and environmental conditions that can be managed by a human driver</td>
<td>System</td>
<td>System</td>
<td>System</td>
<td>All driving modes</td>
</tr>
</tbody>
</table>

http://www.sae.org/misc/pdfs/automated_driving.pdf

© 2016 Synopsys, Inc.
ADAS is Coming to Every Vehicle

99% of vehicles sold in the US (20 OEMs) will offer standard Automatic Emergency Braking by 2022.

Twelve 2017 mid-sized SUVs offer ADAS features, nine of which offer Automatic Emergency Braking.

ADAS-equipped vehicles have fewer collisions and at >20% lower insurance losses for bodily injury and medical payments.
ADAS SoCs Require ISO 26262 Functional Safety Compliance

- ASIL A/B/C/D defines the level of safety; ISO 26262 defines the processes and standards
- Goal is to minimize the susceptibility to random hardware failures by:
  - Defining the functional requirements, applying rigor to the development process, and taking necessary design measures
  - Applying systematic analysis methods
- Compliance certifications for SoCs granted by accredited providers
  - Training, Product & process reviews, Product assessments & certifications

<table>
<thead>
<tr>
<th>Risk potential</th>
<th>QM</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>QM</td>
<td>Not used for safety</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ASIL A</td>
<td>Single-point fault metric &lt; 90% Latent fault metric &lt; 60%</td>
<td>ASIL C</td>
<td>Single-point fault metric $\geq$ 97% Latent fault metric $\geq$ 80%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ASIL B</td>
<td>Single-point fault metric $\geq$ 90% Latent fault metric $\geq$ 60%</td>
<td>ASIL D</td>
<td>Single-point fault metric $\geq$ 99% Latent fault metric $\geq$ 90%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Why Do We Need DRAM in the Automobile?

**MCU**
- Low-to-mid-range CPU
- Realtime OS
- Embedded SRAM
- Medium Density NVM and/or SPI Flash
- 90/65nm moving to 40nm eFlash
- **Requires Functional Safety**

**Infotainment**
- Multimedia CPU + Graphics
- Multiple interfaces: USB, Ethernet AVB, MIPI, HDMI, PCIe, ADC, Sensors, etc
- **Off-chip DRAM** + Embedded SRAM
- SPI Flash, eMMC, other storage
- Security
- 28nm moving to 16nm

**High-End ADAS**
- Multicore CPU + Graphics + EV Accelerators
- Multiple interfaces: LPDDR4, Ethernet AVB, MIPI, HDMI, PCIe, SATA, ADC, Sensors, etc
- **Off-chip DRAM** + Embedded SRAM
- SPI Flash, eMMC/UFS, other storage
- Security
- 16/14nm and shrinking
- **Requires Functional Safety**
Why Do We Need DRAM in the Automobile?

**MCU**
- Low-to-mid-range CPU
- Realtime OS
- Embedded SRAM
- Medium Density NVM and/or SPI Flash
- 90/65nm moving to 40nm eFlash
- **Requires Functional Safety**

**Infotainment**
- Multimedia CPU + Graphics
- Multiple interfaces: USB, Ethernet AVB, MIPI, HDMI, PCIe, ADC, Sensors, etc
- **Off-chip DRAM** + Embedded SRAM
- SPI Flash, eMMC, other storage
- Security
- 28nm moving to 16nm

**High-End ADAS**
- Multicore CPU + Graphics + EV Accelerators
- Multiple interfaces: LPDDR4, Ethernet AVB, MIPI, HDMI, PCIe, SATA, ADC, Sensors, etc
- **Off-chip DRAM** + Embedded SRAM
- SPI Flash, eMMC/UFS, other storage
- Security
- 16/14nm and shrinking
- **Requires Functional Safety**
## DRAM vs SRAM

<table>
<thead>
<tr>
<th>Comparison</th>
<th>DRAM</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type commonly used in new automotive designs</td>
<td>LPDDR4 (discrete die)</td>
<td>Integrated into same die as CPU, or discrete component</td>
</tr>
<tr>
<td>Structure</td>
<td>1 transistor, 1 capacitor per bit</td>
<td>6 transistors per bit</td>
</tr>
<tr>
<td>Cost per bit</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Bandwidth per die</td>
<td>Around 100Gbit/sec per die in automotive applications. Two die are commonly used for 200Gbit/sec.</td>
<td>On-die: theoretically unlimited</td>
</tr>
<tr>
<td>Latency</td>
<td>Typically 15-30ns for most commands, but can be substantially higher depending on previous commands</td>
<td>On-die: few nanoseconds depending on chip construction Discrete component: typically 10ns, deterministic</td>
</tr>
<tr>
<td>Common density per die</td>
<td>4Gbit, 8Gbit</td>
<td>Up to 16Mbit</td>
</tr>
<tr>
<td>Temperature sensitivity</td>
<td>System changes required above 85°C</td>
<td>May operate up to same temperature as CPU (depending on device)</td>
</tr>
<tr>
<td>Reliability features</td>
<td>Susceptible to radiation and soft errors. SoC typically implements error correction for the DRAM</td>
<td>Less susceptible to soft errors. On-die SRAM may have its own error correction.</td>
</tr>
<tr>
<td>Refresh requirements</td>
<td>Requires periodic refresh</td>
<td>No requirement for refresh</td>
</tr>
</tbody>
</table>
**Designing an SoC that Uses DRAM**

*Major Automotive DRAM Concerns*

- Temperature grade (Part of AEC Q100)
  - Grade 2/1/0
  - Necessary power and area trade-offs to reach higher temperature
- ASIL Level for the DRAM interface (ISO26262)
  - ASIL-B with the majority of logic?
  - ASIL-C/D with the CPU?
  - Necessary area and complexity tradeoffs to reach higher ASIL level
  - Certification of the ASIL level
- Demonstrating the ASIL Level to your customer
  - No predefined diagnostics for each ASIL level
  - Certification required
  - What does ASIL B/C/D mean to you?
- TS16949 Quality Management

---

**Customer**

Documentation, Certification

Requirements, Specifications

**Supplier**
How to Choose Automotive DRAM

• Capacity and Bandwidth
• Temperature rating
  – Will the device be in the engine bay, on the windshield, or in the cabin?
  – DRAM Devices are rated by case temperature
• Automotive Qualification
  – AEC Q100, ISO9001/TS16949
• Longevity
  – Will the DRAM be available through the life of the vehicle + long-term spares?
DRAM at High Temperature

• Charge on capacitors in DRAM devices leak
  – Function of temperature
  – Contents need to be refreshed periodically (normal operation of DRAM)

• Computing DRAM devices often designed for 64ms refresh interval
  – Based on worst cell of all – out of Billions of cells in LPDDR4 devices

• Charge degradation is significant at 85°C
  – Increased refresh rate required
    – Reduces bandwidth
    – Increases power & die heating

• Manufacturers are releasing DRAM with higher temperature ratings
  – Up to 125°C case temperature
  – “Secret Sauce” among manufacturers
    – Different circuit techniques for 125°C operation
    – LPDDR4 standard allows “efficient data protection schemes based on larger data blocks”
High Temperature DRAM Solves One Problem of Many

- Cosmic Particles
- Metastability
- Row Hammering
- Retention Fault
- Silicon Aging
- Signal Integrity
- Coupling Fault
- Etc…
- Radioactive Decay
- ISI, X-TALK, SSO
- Stuck-at Fault
- High Temperature

Error Correcting Codes (ECC) are still needed on the DRAM bus!
Best Arrangements of DDR4 for Automotive

- Workloads with a lot of images and video lend themselves to 16-bit and 32-bit channels
- DDR4 has a Command/Address bus that is designed to fan out to multiple DRAM devices
- Adding sideband ECC to DDR4 is not difficult since 4-bit and 8-bit wide DDR4 devices are readily available
Some Arrangements of LPDDR4 for Automotive

- Workloads with a lot of images and video lend themselves to 16-bit and 32-bit channels

- LPDDR4 has a Command/Address bus that is designed to be point-to-point
  - Multidrop to 3 or 6 devices is problematic from a loading and PCB routing perspective

- Adding sideband ECC to LPDDR4 is difficult – standard calls for 16-bit wide LPDDR4 devices
  - More than half the ECC memory is unused in sideband ECC Configuration
LPDDR4 ECC Solution: In-line (In-band) ECC

- In-line ECC allows data and ECC to be stored together in the same DRAM
  - Uses some of the DRAM bandwidth and capacity to store ECC
    - But more efficient use of capacity than using a X16 device for sideband ECC
  - Adds some latency
  - Protects against both DRAM bit errors and data transmission bit errors
  - Recommended solution for systems requiring LPDDR4 and ECC
    - Add additional busses if more bandwidth needed
One of many possibilities… Convert one ECC memory into an in-line data+ECC memory to recover 25% bandwidth – same number of DRAM dies, few more pins, slightly more area than sideband ECC.
Command/Address Parity (DDR4)

- Protects against signal integrity errors on the Command/Address bus
  - Command type incorrect or command sent to incorrect address
- DDR4 Devices and some DIMMs have command/address bus parity detection and alert
  - Allows system to detect error
  - Some systems may retry after error
  - DDR4 parity function adds Latency
- No CA Parity function on LPDDR4 devices… but some options
Cyclical Redundancy Checks (DDR4)

- Protects against errors on writes
  - Single bit errors correctable by Hamming ECC unless a second error occurs in the same word due to other effects
- DDR4 Devices have optional Cyclical Redundancy Check (CRC) on write data
  - CRC Polynomial detects 1 bit, 2 bit, and some multi-bit errors
  - Allows system to detect error (and retry for bonus points)
- No equivalent function on LPDDR4 devices
Mitigating Bit-Flips on the SoC

- Radiation affects more than DRAM bit-cells
- Any flop or SRAM bit-cell on small-geometry processes can be affected
- Protect on-chip memories with ECC
- Protect datapaths with parity or ECC
- Mitigate potential bit-flips using diversity or redundant hardware
Metastability Mitigation

• DDR Interfaces often have clock domain crossings (CDC)
  – On-Chip Bus to memory controller, or between DRAM and DFI
• Consider CDC Synchronization with multiple stages
  – Improves Mean Time Between Failure (MTBF) / Failure in Time (FIT)
  – Makes latency worse
• Choose library cells with better metastability resistance
Securing the DRAM Interface

- The DRAM bus is an opportunity for hackers:
  - Theft/copying of proprietary code
  - Unintended operation of vehicle
- Secure the DRAM bus directly with scrambling or encryption
- Secure the register bus to privileged code only
- Secure the on-chip bus – no unprivileged code accessing privileged areas
# ISO 26262 Certified IP Safety Package Deliverables

<table>
<thead>
<tr>
<th>Safety Package Deliverables</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>FMEDA</td>
<td>Safety Manual</td>
</tr>
<tr>
<td>ASIL X Ready Certificate</td>
<td>ASIL X Ready Certification Report</td>
</tr>
</tbody>
</table>

## Additional ISO 26262 Work Products

<table>
<thead>
<tr>
<th>Additional ISO 26262 Work Products</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Document Management Plan</td>
<td>Hardware Safety Req Spec</td>
</tr>
<tr>
<td>Documentation Guidelines</td>
<td>Safety Plan</td>
</tr>
<tr>
<td>Safety Process Rules</td>
<td>Verification Plan</td>
</tr>
<tr>
<td>Quality Management System (QMS) Overview</td>
<td>Verification Reports</td>
</tr>
<tr>
<td>Evidence of Field Monitoring</td>
<td>Change Management Plan</td>
</tr>
<tr>
<td>Configuration Management Plan</td>
<td>Change Request</td>
</tr>
<tr>
<td>Product Operation Service Decomm Reqs</td>
<td></td>
</tr>
</tbody>
</table>

Provided upon request or during safety audits.
HW Design & Verification Flow
ISO 26262 Ready IP

DesignWare IP Safety Design & Verification Flow

Systematic Failure Based Verification
- FPGA/Test chip System IP Validation/Emulation
  - Verification IP - Embedded SW

Random Failure Analysis (ISO 26262)
- Methodologies – Safety Goals & Requirements Analysis, FMEDA
- Coverage Metrics – Fault Coverage
- Related Tools – Certitude or VCS used for Fault injection used for fault coverage analysis for FMEDA report

SoC Architecture

Top-Down Design Spec Driven Verification Planning

Core Specification

Digital Specification

HW Safety Features

Design Implementation

RTL Design

FIT Rate Analysis

HW Safety Goals

HW Safety Requirements

IP/SoC Level Verification

Validation

Safety Manual

FMEDA Report

Fault Injection/Coverage Analysis

Bottom-up Coverage Closure

FPGA

ASIC

Module Design Verification

Fault Rate Analysis

HW Safety Features

Product Level Development
- Methodologies – CDV, UVM
- Coverage Metrics – Functional, Code, Lint & Build Coverage

Module Level Development
- Methodologies – CDV, UVM, Formal/Dynamic
- Coverage Metrics – Functional, Code, Lint & Build Coverage
Protocol Verification Challenges

**Complexity & Size**
Exponential Verification Complexity

**Performance**
Number and Length of Tests

**Domain Knowledge**
Protocols Evolve and Emerge

**Integration**
Testbench/VIP
Languages & Methodologies

**Debug**
Signal to Protocol

**Coverage**
Lack of Complete solution for Planning and Coverage
Memory VIP Architecture

Extends Next-Generation Architecture

Accelerated Verification
- Native SystemVerilog/UVM
- No wrappers

Memory Configuration
- Random configurable
- Select by vendor part #
- Select by individual attribute
- Configuration Creator GUI

Protocol Checks
- Validated with Synopsys Controller & PHY

Accelerated Easy Debug
- Verdi protocol aware debug
- FSDB trace files

Accelerated Verification Closure
- Built-in coverage
- Verification plan
Conclusions

• ADAS offers a significant improvement in vehicle safety
• ADAS is coming to new vehicles soon – and autonomous driving not long after
• DRAM is arriving in safety-critical applications within ADAS and autonomous driving
• Select DRAM for Bandwidth, Capacity, Temperature Rating, and PCB integration
• The DRAM interface needs to be designed with:
  – Functional safety to reach the required ASIL level B, C, or D
    – Safety features
    – Design methodology
    – Verification
  – Temperature requirement to meet AEC Q100 Grade 2/1/0
• The DRAM interface should be secured to prevent tampering

• Synopsys provides automotive-qualified IP, verification, and tools for automotive designs
Thank You

Marc Greenberg
Director, Product Marketing, DDR and AMBA IP
Synopsys
marc.greenberg@synopsys.com