Configurable Mixed-signal ICs & Power Sequencing

Mike Noonen

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2016
What I Will Cover Today

• Introduction To Configurable Mixed-signal ICs
• Non-volatile Memory Used For Mixed-signal
• Overview of Silego CMIC Platform
• CMIC Power Sequencing Techniques and Application Examples
• DDR4 Power Sequencing Example
• Summary
Introduction to Configurable Mixed-signal ICs
Silego is the Pioneer & Leader in Configurable Mixed-signal IC Solutions for Mass Markets

- DESIGN IN MINUTES
- PROTOTYPE IN DAYS
- PRODUCTION IN WEEKS
Silego’s Key Technologies Are Built Around Configurable Silicon

- Leading CuFET Technology
- Ultra Low Power Timing
- Analog and Digital Blocks
- Graphical Design Tool and Development Kits
- Flexible Manufacturing
The Silego Configurable Mixed-Signal Solution

CMIC Platform

Delivery Model

Interactive Design Support

Instant Prototyping

Cost Optimized Flexible Manufacturing

Differentiated Products

Improved Time To Market

Small Low Power Reusable

10/13/2016
Configurable Mixed-signal IC Can Address Many Functions, Applications and Markets

Functions
- Finite State Machine
- Timing Delays
- Counters
- Pulse Width Modulator
- Comparators
- Voltage Monitor
- Voltage Reference
- ADC
- Glue Logic
- Level Shifter

Motor & Fan Control
- System Reset
- LED Control
- Over Voltage Protection
- Power Sequencing
- Voltage Detection
- Frequency Detection
- Sensor Interface
- Port Detection
- Temperature Control

Handheld Devices
- Wearable Electronics
- Computing & Storage
- Consumer Electronics
- Smart Home
- Networking & Communications
- Medical
- Industrial

Applications

Markets
Integrate Analog and Digital
Implement complete functions in one device as small as 1.6 x 1.6 mm

Shrink Footprint
Fewer components and less routing complexity

Reduce Power Consumption
Extend battery life by powering fewer discrete devices and dynamically managing power within the GPAK

Adapt
Adapt to changing requirements quickly and create new samples in minutes

Fast Time to Market
Easy-to-use GPAK development hardware and GPAK Designer software
Configurable Mixed-Signal Market Position

No Direct Competition In Configurable Mixed-Signal ICs
Design and program samples on your desktop in minutes
- Quick-turn manufacturing can produce thousands of samples in a few days

Fix problems/bugs on other devices on your board
- GPAK provides flexibility to adapt to unforeseen requirements during development
One-Time Programmable Non-Volatile Memory Used for Mixed-signal
EM773 is an ARM Cortex-M0 based, low-cost 32-bit energy metering IC.

“EDN Analog Product of the 2011”

Old World Analog
Simple, Bipolar, Unintelligent

New World Mixed-Signal
Complex, Analog + Digital, Connected, Intelligent, CMOS
There Are Many Opportunities to Add NVM Intelligence & Value To Mixed-Signal

Configuration, Sequencing
Code Execution
Code Storage
Trim, Calibration
Personalization
Field Programmability
There Are Many Non-Volatile Technologies

<table>
<thead>
<tr>
<th>Memory Technology</th>
<th>eFLASH</th>
<th>ROM</th>
<th>eFUSE</th>
<th>CMOS FG (OTP)</th>
<th>CMOS FG (FTP)</th>
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<td>Code Storage, Configuration, Analog trim, Patches, Encryption</td>
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</table>

Source: Kilopass
Where Available, eFLASH Is Expensive

Typical FLASH NVM Process + Design Royalty
Macro < 8Mb

Year 1: 9%
Year 2: 8%
Year 3: 6%
Year 4: 4%
Year 5: 3%

Plus Additional Process Cost & Complexity
GlobalFoundries BCDlite™: Modular Process Architecture

- 1.8V ULL or 1.8V IC w/ OTP
- 10,12,16,20,24, 35V LDMOS
- Low Rdson 7-10V NMOS
- 30V LDMOS
- 60V LDMOS
- HRES
- MIM Cap
- Zener Diode
- TaN Resistor
- 10V LDMOS, Schottky Diode, VNPN, VNP, MOS Cap, Varactor, OTP
- 5V or 6V Process
- OTP
One Time Programmable Is Sufficient For A Variety of Applications and Functions

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<tr>
<th>Function → Application</th>
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<th>Parameter Setting</th>
<th>Encryption</th>
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Source: Kilopass
Anti-fuse One-Time Programmable NVM Is A Good Balance Between Cost and Capabilities

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Anti-Fuse Technology

Dielectric that prevents current flow
Applying a voltage melts the dielectric
IC Design with Multiple Options: Pinout, Voltage, etc.

Reticle Patterned With This IC Design

Multiple Benefits
- 1 reticle instead of 20-30
- Reduced design variation – higher yield
- Reduce Inventory
- 100% Sell through
- Reduced cycle time & time to revenue for the right product

When An Order Comes In, Personalization Can Happen Here

Fab

Assembly & Test

Die Bank

Distribution

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Configurable Mixed-signal IC Architecture & Design Flow
GreenPAK 5 Configurable Mixed-signal IC Family

SLG46532

GreenPAK 5
Dual-Supply Programmable Mixed Signal Matrix

Features
- Logic & Mixed Signal Circuits
- Highly Versatile Macro Cells
- Read Back Protection (Read Lock)
- 1.8 V (±5%) to 5 V (±10%) VDD
- 1.8 V (±5%) to 5 V (±10%) VDD2 (VDD2 ≤ VDD)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch

Applications
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration

STQFN-20 (Top View)
GreenPAK 5 CMIC
A Wide Variety of Analog & Digital Resources

Four Analog Comparators (ACMP)
Two Voltage References (Vref)
Seventeen Combination Function Macrocells
  • Three Selectable DFF/Latch or 2-bit LUTs
  • One Selectable Continuous DFF/Latch or 3-bit LUT
  • Four Selectable DFF/Latch or 3-bit LUTs
  • One Selectable Pipe Delay or 3-bit LUT
  • One Selectable Programmable Function Generator or 2-bit LUT
  • Five 8-bit delays/counters or 3-bit LUTs
  • Two 16-bit delays/counters or 4-bit LUTs
State Machine
  • Eight States
  • Flexible input logic from state transitions
Serial Communications
  • I2C Protocol compliant

Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
Programmable Delay
Additional Logic Functions
  • Two Deglitch Filters with Edge Detectors
  • One Inverter
Two Oscillators (OSC)
  • Configurable 25 kHz/2 MHz
  • 25MHz RC Oscillator
Crystal Oscillator
Power-On-Reset (POR)
Eight Byte RAM + OTP User Memory
  • RAM Memory space that is readable and writeable via I2C
  • User defined initial values transferred from OTP

10/13/2016
GreenPAK CMIC Design Flow

Product Definition

Customer creates their own design in GreenPAK Designer

Emulate design to verify behavior

Program Engineering Samples with GreenPAK Development Tools

Customer verifies GreenPAK in system design

GreenPAK Design approved

E-mail design file to GreenPAK@silego.com

E-mail Product Idea, Definition, Drawing, or Schematic to GreenPAK@silego.com

Silego Applications Engineers will review design specifications with customer

Samples and Design & Characterization Report sent to customer

GreenPAK Design approved

Customer verifies GreenPAK design

GreenPAK Design approved in system test

Custom GreenPAK part enters production
Silego Technology’s GreenPAK Designer development software enables a completely graphical design process, requiring no programming language or compiler allowing a designer to configure, program, and test custom GreenPAK samples in minutes.

- Schematic capture-like design and routing
- Entire component library showing available resources for each device
- Easy component configuration
- Example projects and support documentation
GreenPAK Designer Launcher User Interface

SLG46536V

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<th>Max. CNT/DLY</th>
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**Details**

**Package:**
STQFN-14L

**Description:**
The SLG46536V provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macro cells of the SLG46536V. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macro cells in the device include the following:

- Four Analog Comparators (ACMP);
- Two Voltage References (Vref);
- Twenty-four Combination Function Macrocells:
  - Three Selectable DFF/Latch or 2-bit LUTs;
  - One Selectable Continuous DFF/Latch or 3-bit LUT;
  - Twelve Selectable DFF/Latch or 3-bit LUTs;
  - One Selectable Pipe Delay or 3-bit LUT;
  - One Selectable Programmable Pattern Generator or 2-bit LUT;
  - Five 8-bit delays/counters or 3-bit LUTs;

**Datasets:**
- Datasheet
- Product page
- Application notes
- Get samples
- Contact us

**User Guides:**
- New
- Open
- Close
Schematic Capture Supporting Complex Designs
Comprehensive Rules Checking
Design Emulator

Using the included GreenPAK design emulator, designers can test their project in the development environment, no soldering required.

- In-circuit testing
- Make real time design changes
- Test and Debug Tools
  - Signal generator
  - Virtual buttons
  - LEDs
Built-in Signal Generator
GreenPAK Development Board
CMIC Power Sequencing Techniques and Application Examples
• So can powering one off.
• Timing, order of events, and power levels need to be just right for proper system functionality and stability.
• Power sequencing can also prevent unnecessary current draw while portions of the design sit idle, waiting for prerequisite systems to be powered.
• Some SoCs and FPGAs may require more than ten rails, which if sequenced using discrete components, could introduce extra power and board space overhead.
 Configurable Mixed-signal Makes Power Sequencing Easy

- Using Silego’s GreenPAK™ family of devices, it is easy to implement custom power sequencing designs in an extremely small area, using minimal power and board space.
- When paired with the tiny, ultra-low RDSON GreenFET™ Integrated Power Switch, power sequencing with Silego is an incredibly efficient solution.
- Often in various combinations in a single system, some common methods for power sequencing include:
  - Fixed Delay Sequencing
  - I2C Acknowledge
  - Voltage Sensing
  - Power Good
CMIC Power Sequencing Benefits

- **System Stability**
  - Zero Code - Implementing features in hardware ensures stability
  - Can integrate many components ensuring fewer points of failure

- **Power Consumption**
  - Low-power - Can operate continuously without ruining power budget

- **Size**
  - Small as 1.2 mm²

- **Flexibility**
  - GPIO are configurable - Pull-up/down resistors, Push-Pull, Open drain, etc.
  - GPIO routing is flexible – Ensuring the least complexity in PCB routing
  - Integrates many common components – Generate custom timing and logic to fit the requirements of many power sequencing designs
• One method for sequencing multiple sub-systems is to allot a fixed amount of time for each start-up sequence.
• This is appropriate for systems which do not feature a Power Good signal.
• Finding a discrete solution with the exact delay timings needed can take hours, but with GreenPAK’s configurable logic and timing resources, developing a custom system is easy.
Key Design Considerations

• Delay Time – Using GreenPAK’s internal oscillators and CNT/DLY blocks, it is possible to address a wide range of timing requirements

• ON Signal Polarity – GreenPAK can be configured to output active high or low using integrated inverters and LUTs
I2C Acknowledge

- Another option in programmable systems with I2C is to send a command to the power sequencer, in this case GreenPAK, to let it know start-up was completed successfully.

- Using GreenPAK's I2C virtual inputs, it is easy to treat an I2C command just like a digital Power Good signal.
I2C Acknowledge

Key Design Considerations

- **I2C Speed** – GreenPAK I2C supports up to 400 kHz

- **I2C Address** – GreenPAK can have up to 16 unique I2C addresses
• To ensure system stability, many SOCs and FPGAs require a minimum voltage for startup.

• Monitoring the power level of a rail can be done simply using GreenPAK’s configurable analog comparators.
Key Design Considerations

- **Over-voltage/Under-voltage Threshold**
  Supply tolerances vary, but using GreenPAK with integrated ACMPs enables reliable sequencing over a wide range of user specified conditions.

- **Time Sensitive Voltage Limits** – Varying periods of voltages outside the limit may be tolerable for some systems. GPAK’s configurable CNT/DLY blocks can be used to reject reset events below a wide range of time thresholds.

- **Hysteresis** – Nominal voltage requirements may incorporate hysteresis. GPAK’s ACMPs can be configured with 25, 50, or 200 mV hysteresis.
Many ICs have the ability to produce a Power Good (PG) signal once the respective systems have finished their start-up routine. This can be useful in systems where start-up time is not fixed and may depend on multiple variables.
Key Design Considerations

- **ON and PG Signal Polarity** – GreenPAK can be configured to output active high or low using integrated inverters and LUTs.
Power Good Logic Example

Discrete Before

CMIC After

10/13/2016
## Power Good Logic Example

### Discrete Before

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Desc.</th>
<th>QTY</th>
<th>X</th>
<th>Y</th>
<th>Area mm²</th>
<th>Unit</th>
<th>Total</th>
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<td>3</td>
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| Layout Efficiency | 70% | 79.71 |
| Placement Cost    | $0.01|
| Total Cost        | $0.54|
CMIC Delivers Significant Savings

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<th>Component Type</th>
<th>Desc.</th>
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<th>Y</th>
<th>Area mm²</th>
<th>Unit</th>
<th>Total</th>
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Layout Efficiency: 70% (9.29)

Placement Cost: $0.000

Total Cost: $0.191

CMIC Area Savings vs Discrete: 88%

CMIC Cost Savings vs Discrete: 66%
CMIC Design Example
Basin Falls Power Supply Sequencing
PMIC and EC replacement
Basin Falls Platform

Skylake-X (~140W)
• 6C up to 10C
• Up to 44 Lanes PCIe3.0

Kaby Lake-X (~112W)
• 4C only
• Up to 16 Lanes PCIe3.0

Skylake-X: 4 Channels DDR4
• 2667 1DPC
• 2400 2DPC
• UDIMM non-ECC

Kaby Lake-X: 2 Channels DDR4

DMI 3.0 x4
PMIC and EC power sequencing, Power Good, RESET and FET driver control signals:
• DPWROK and RSMRST_N
• DDR Source rail Sequencer and FET Driver
• ALL_SYS_PWRGD, PCH_PWROK, SYS_PWMOQ
• DDR Rail Sequencing
DDR Rail Sequencing

Original Schematic

Date: 10/13/2016
Sequencing of +V5, V12, DDR Generation

REF: Basin Falls

10/13/2016
Sequencing of DDR Rails

REF: Basin Falls

10/13/2016
DDR Rail Sequencing Design using Silego CMIC GPAK
DDR Rail Sequencing Design using Silego CMIC GPAK
## Power Sequencing Discrete vs CMIC Implementation

### Discrete Implementation

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<th>Pricing</th>
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<td>Cost ($ ea.)</td>
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<tr>
<td>ACMP's</td>
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<tr>
<td>Delays</td>
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<tr>
<td>LUTs / DFFs</td>
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### CMIC Implementation

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<table>
<thead>
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<th>Silego Area Calculations</th>
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<tr>
<td>Part Number</td>
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<tr>
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## Power Sequencing Discrete vs CMIC Implementation

### Discrete Implementation

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<tbody>
<tr>
<td></td>
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<td>Delays</td>
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<td>LUTs / DFFs</td>
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<tr>
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### CMIC Implementation

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</table>

### CMIC Volume Pricing $0.20
CMIC Delivers Significant Board, Cost & Time Savings

CMIC Area Savings vs Discrete: 56%
CMIC Cost Savings vs Discrete: 86%
Conclusions & Summary

- Configurable Mixed-signal ICs Are Possible with the Clever Combination of NVM, Circuit Design And Software

- OTP NVM Offers The Right Mix Of Cost And Capability For CMIC Applications

- Power Sequencing Has Many Flavors And Can Be Complex

- CMICs Can Improve Power Sequencing Design By Saving Development Time, Cost And Board Space
Designing with Silego CMICs becomes the de-facto industry standard

Silego leads the paradigm shift from mixed-signal circuit design on PCBs with discrete components to CMICs

Enable our customers to bring their products to market faster, consume less power, require less space and be more cost effective

Thank You