Emerging Memory: In-System Enablement

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Background

- There is an emergence of new memory technologies currently
- The industry needs a way to evaluate and understand system level implications (persistence, latency, etc)
- In-system evaluation platform for current and developing memory technologies needed
- System enablement allows for more accurate, user/application oriented, development and evaluation

Challenges

- Adaptable solution for maximum flexibility
- At speed memory bus operation with high bandwidth to and from processor
IBM’s POWER memory architecture achieves high memory bandwidth per processor

- The existing dedicated memory buffers (ASICs) do not have all the flexibility one would want to enable different memory technologies

- The different characteristics for STT-MRAM, PCM, ReRAM require a more flexible interface to enable in-system functionality
Primary Challenge

a. Keep much of the existing memory buffer functions shown above
b. Add flexibility for the requirements around new memory technologies

Answer = An “at-speed”, full function FPGA card on IBM’s DMI Bus. Aka “Con Tutto”
- 8 DMI links available on a P8 Dual-Chip-Module
- Differential Memory Interface (DMI) high-speed links connect to a memory buffer ASICs
- 4 memory controllers per memory buffer ASIC
- ASIC and DRAM chips are co-located on a custom DIMM (CDIMM)
- 32 memory controllers available to P8
- Built an FPGA-based card that plugs into the DMI slot
- Enables regular system operation with any mix of CDIMMs and ConTutto cards populated
- Full compatibility with DMI protocol
- Memory controllers implemented in fabric logic and independent of DMI protocol logic
- Flexible system architecture enables easy implementation of additional features
Centaur DIMMs
ConTutto – Prototyping Platform

Joint IBM Systems Group and IBM Research project

- 4 high speed lanes
- 240pin memory sockets
- Large FPGA with capacity for additional functions
- Connection to service processor
- Differential Memory Interface Connector

- **Prepare for Future Memories**: Enable MRAM, PCM, RRAM on the P8 memory bus
- **Evaluate NVDIMMs**: Bringup in Power systems, functionally evaluate
- **Innovate**: Enable industry and OpenPOWER partners to innovate on the P8 Differential Memory Interface link

Note: This is a prototyping platform, not a product
Contutto Plugged into IBM Power S824L

- Main Memory
- Power Supplies
- Power8 Processors
- Con Tutto Card
- High Speed Fans
ConTutto – Side view plugged into an IBM Power S824L
Early latency results using FIO with our Beta level Kernel Driver in POWER8 System

- NVDIMM-N and STT-MRAM have similar performance with Con Tutto on DMI
- DMI/Memory bus is the lowest latency attach point versus NVMe/PCIe
- FIO – Flexible IO Benchmarking
- Early IOPS results using FIO with our Beta level Kernel Driver in POWER8 System
- Improved IOPS on the Memory bus is a reality
- Testing with higher iodepth and numjobs ongoing
Future Activity

- Optimize Kernel driver for persistent memory support and performance
- Ensure pmem aware applications run transparently on POWER systems
- Continue to partner with memory suppliers on new technologies
- Migrate to DDR4 interface and socket at the appropriate time
Getting involved and more information

http://openpowerfoundation.org/
http://openpowerfoundation.org/presentations/contutto/
http://openpowerfoundation.org/presentations/programmable-near-memory-acceleration-on-contutto/